

FIG.1

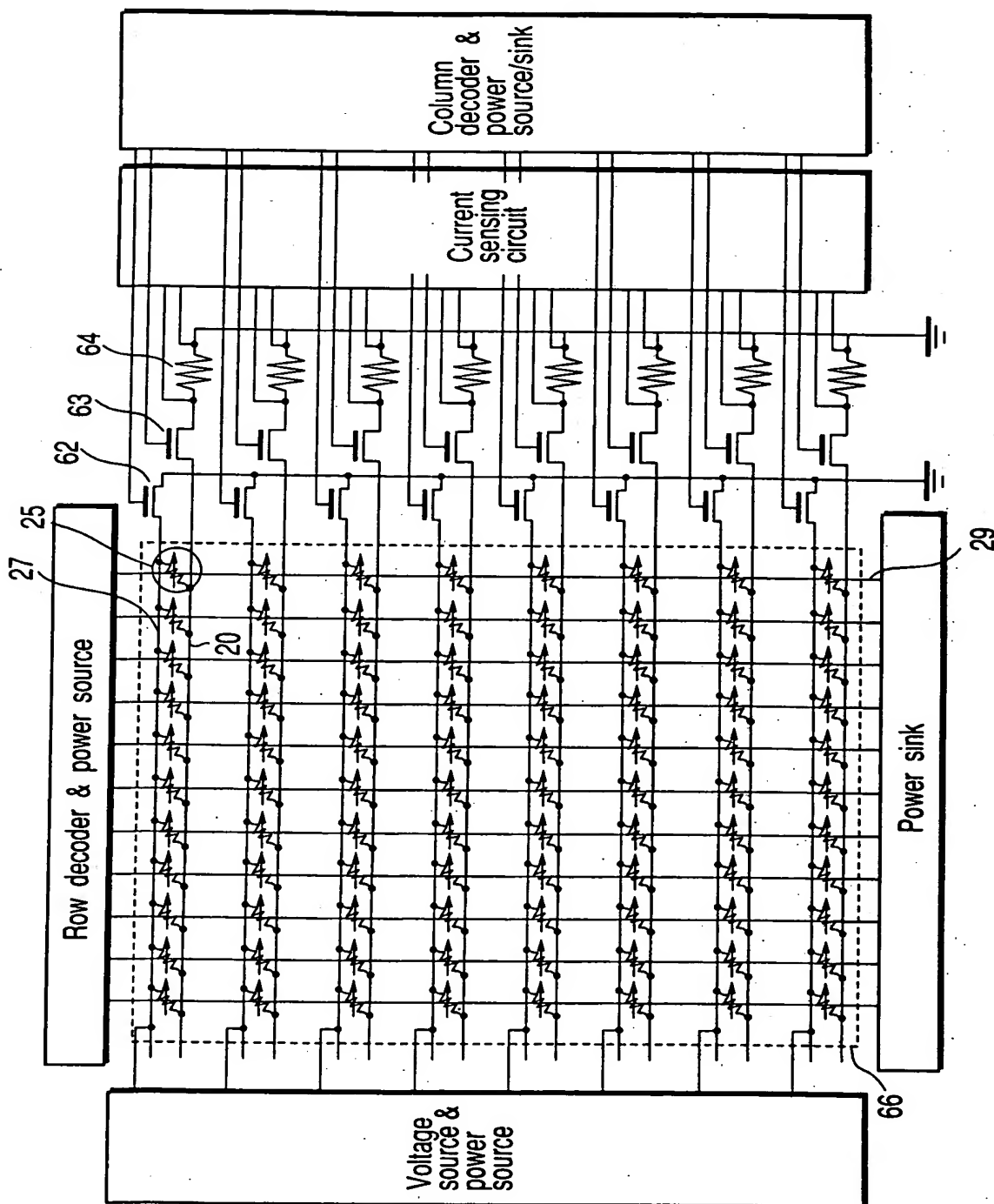


FIG. 2

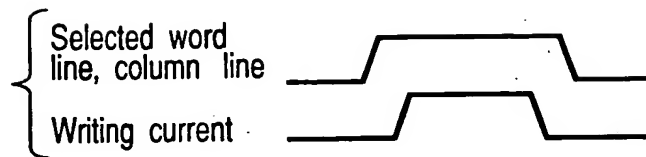


FIG. 3

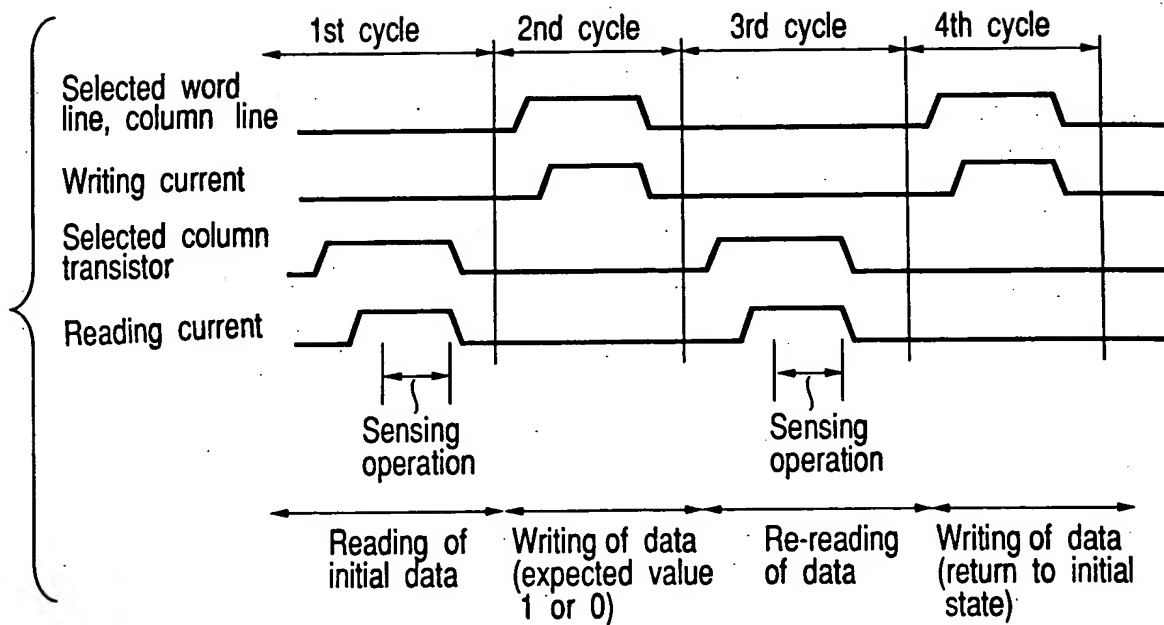


FIG. 4

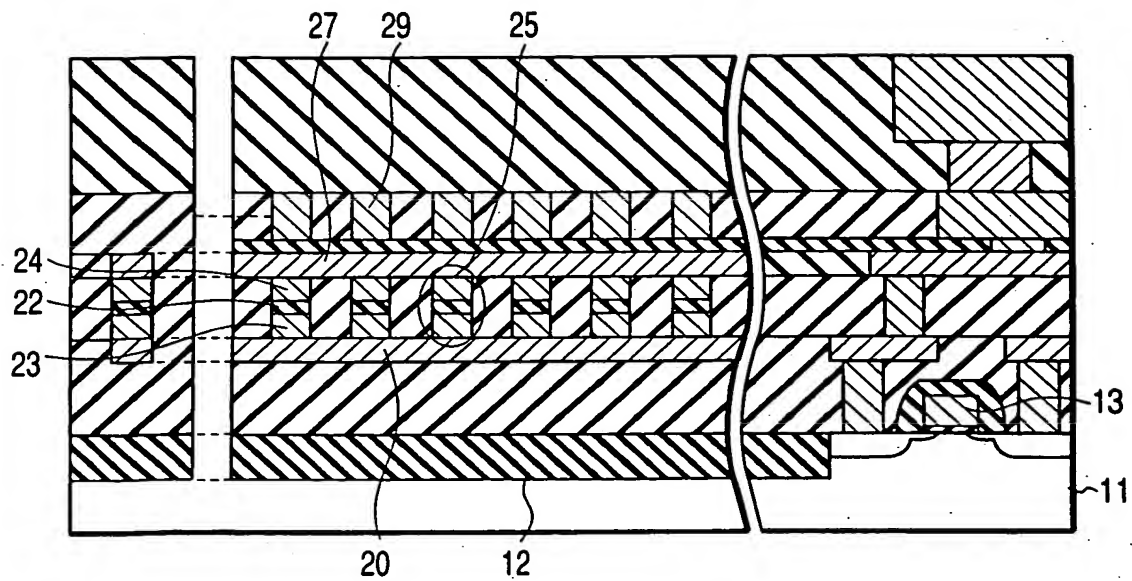


FIG. 5

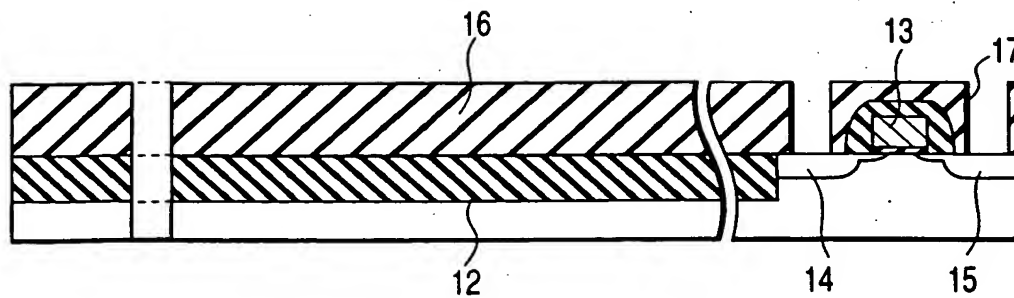


FIG. 6

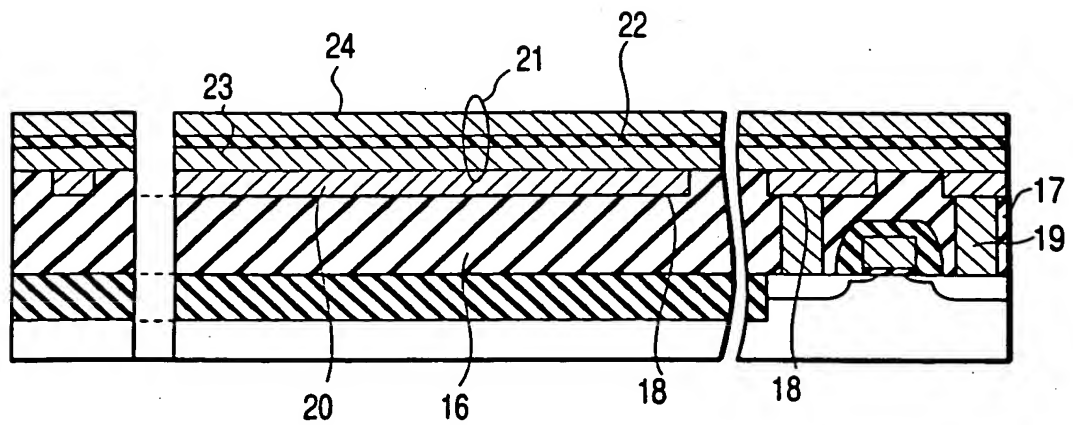


FIG. 7

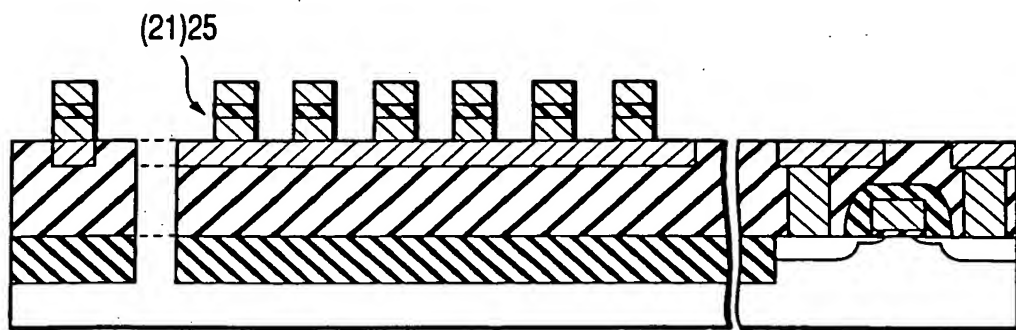


FIG. 8

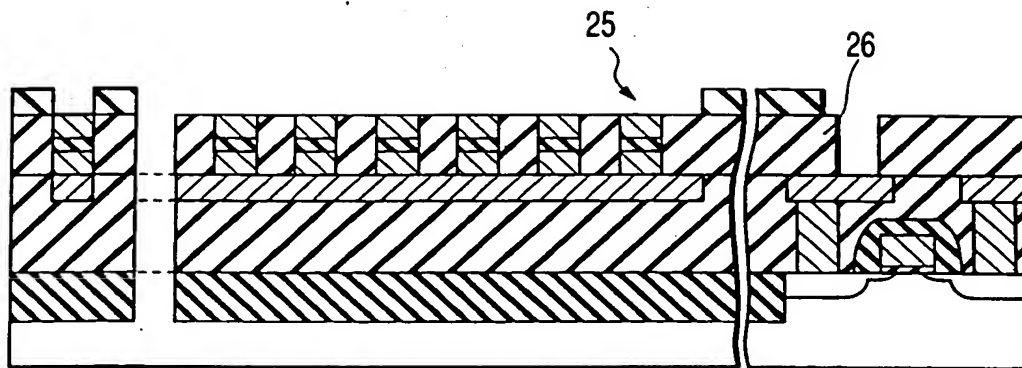


FIG. 9

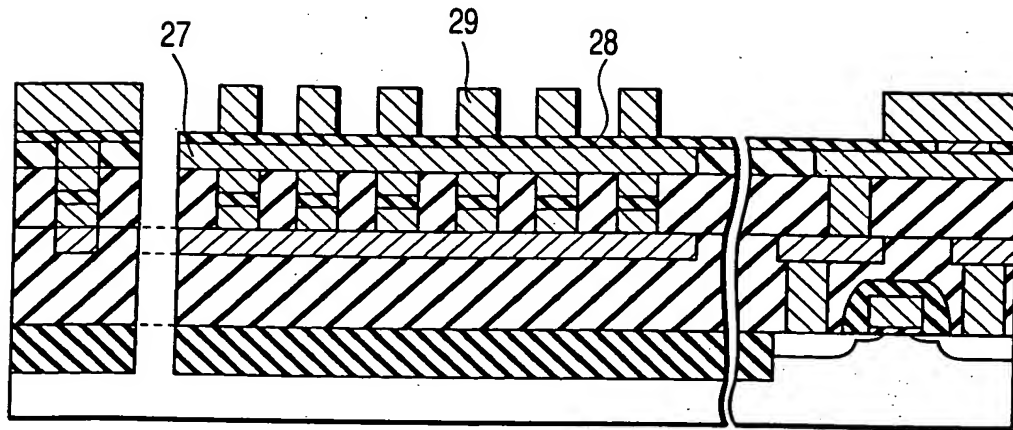


FIG. 10

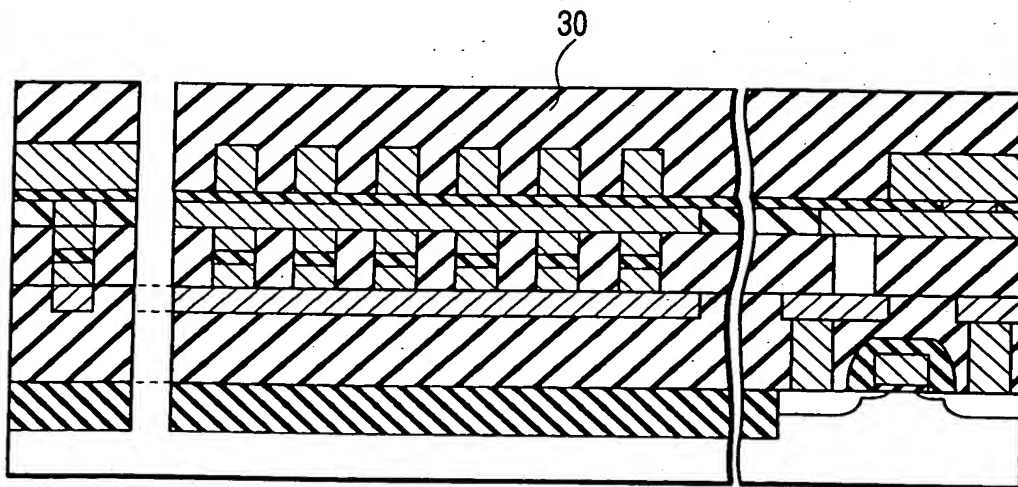


FIG. 11


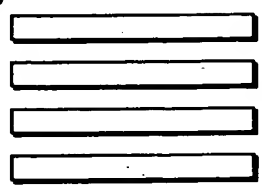
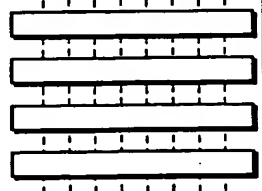
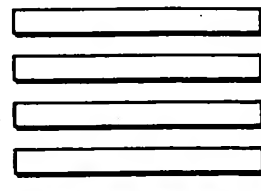
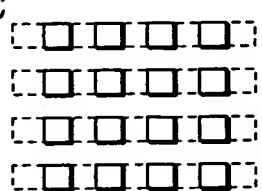
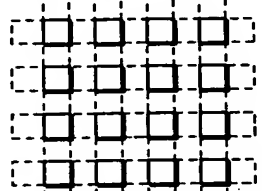
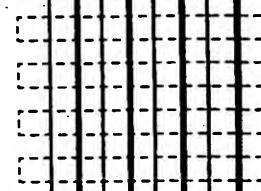
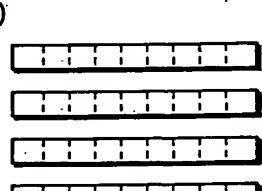
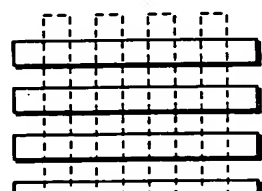
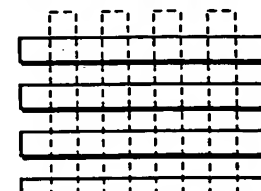
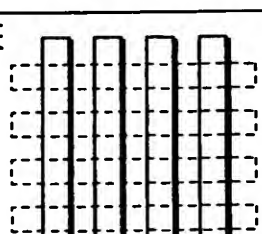
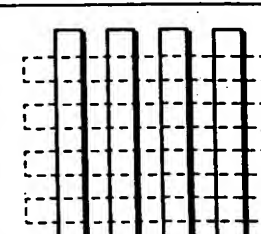
	1st Embodiment	2nd Embodiment	3rd Embodiment
Gate electrode (A)	1-A	2-A 	3-A
Lower data transfer line (B)	1-B 	2-B 	3-B 
TMR (C)	1-C 	2-C 	3-C 
Upper data transfer line (D)	1-D 	2-D 	3-D 
Word line (E)	1-E 	2-E	3-E 

FIG. 12

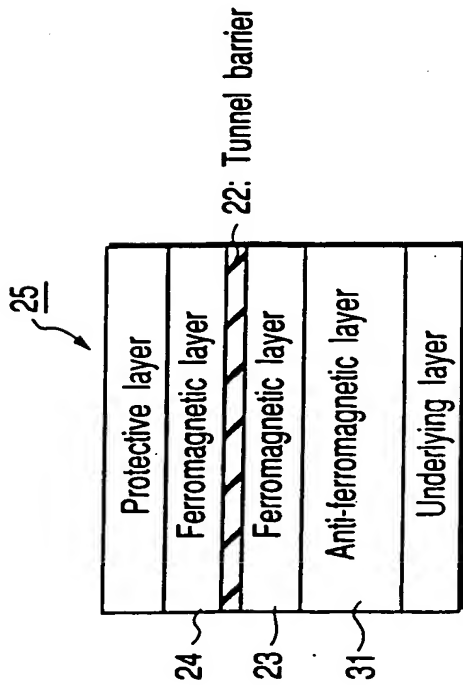


FIG. 13A

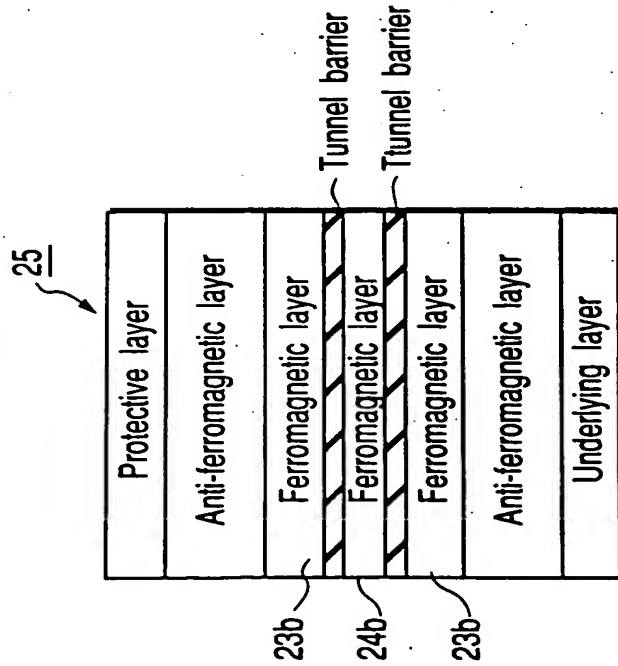


FIG. 13C

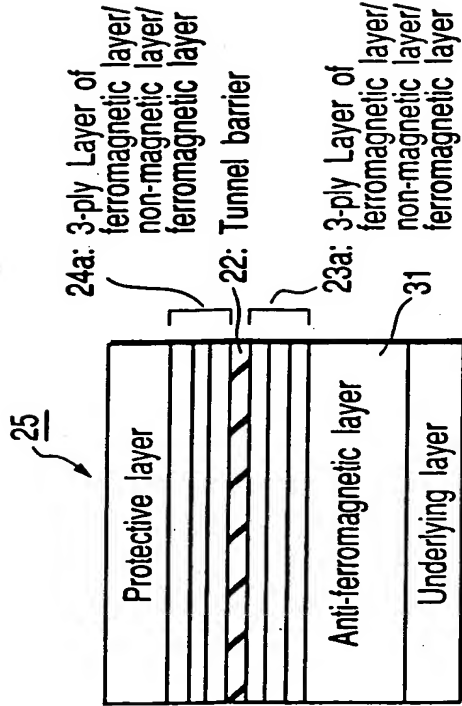


FIG. 13B

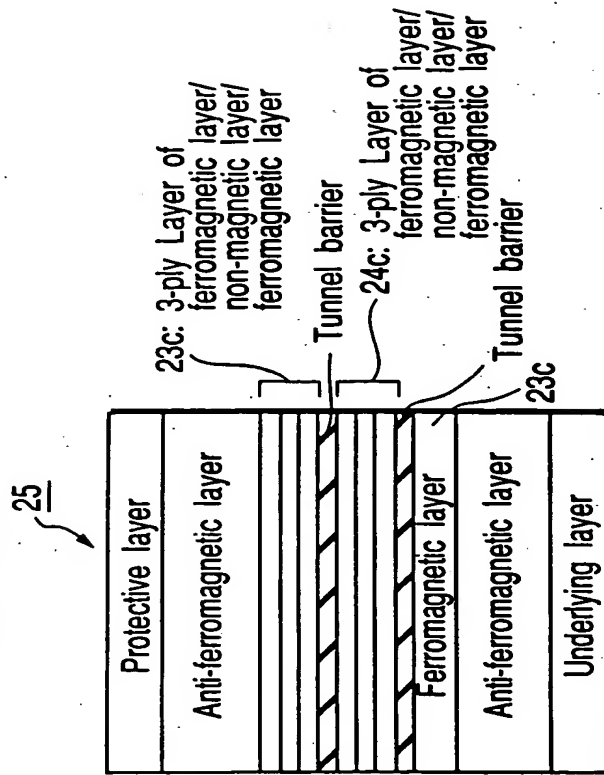


FIG. 13D



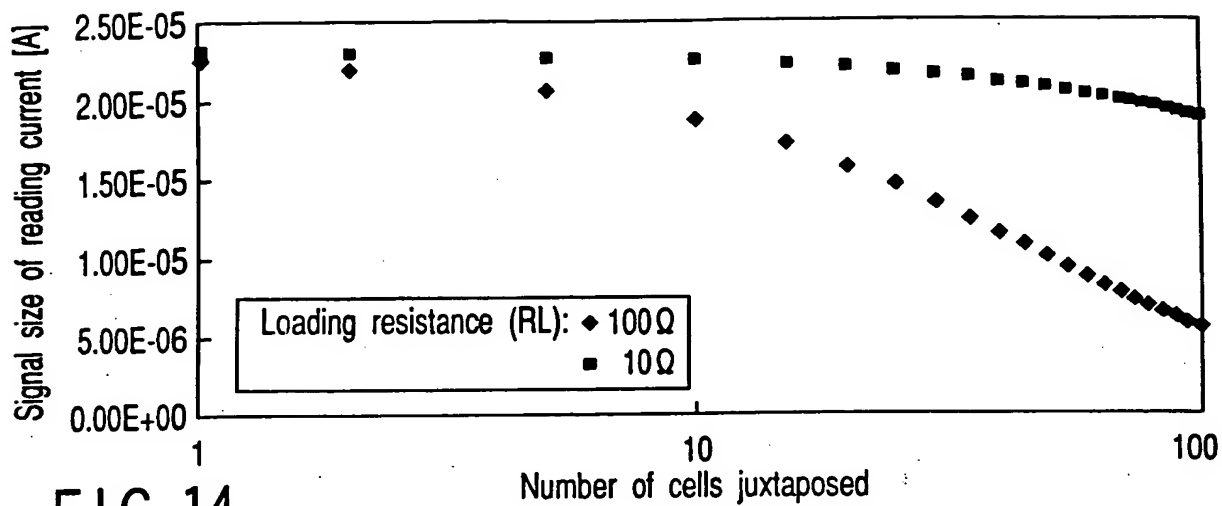


FIG. 14

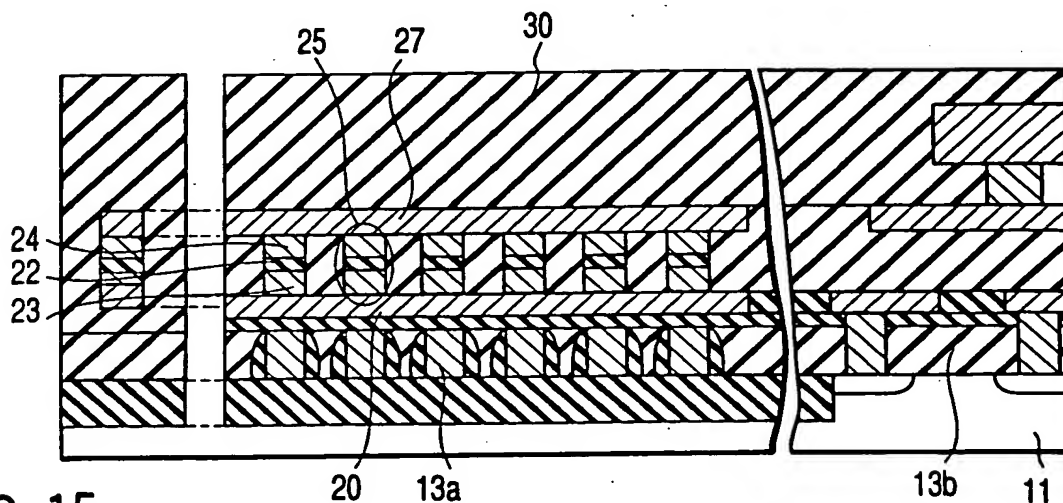


FIG. 15

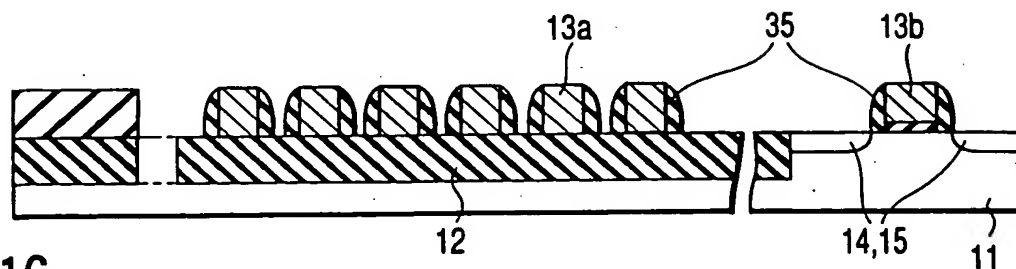


FIG. 16

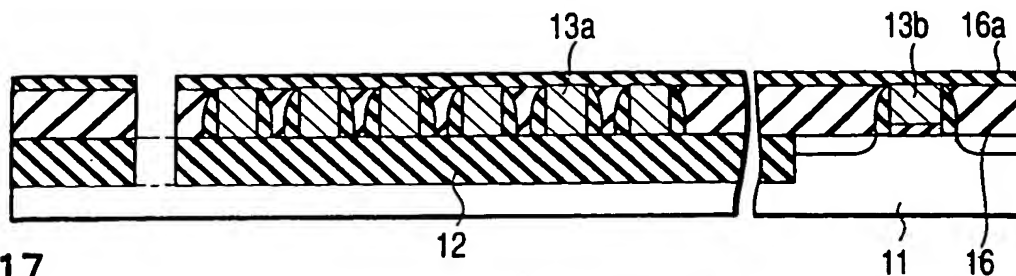


FIG. 17

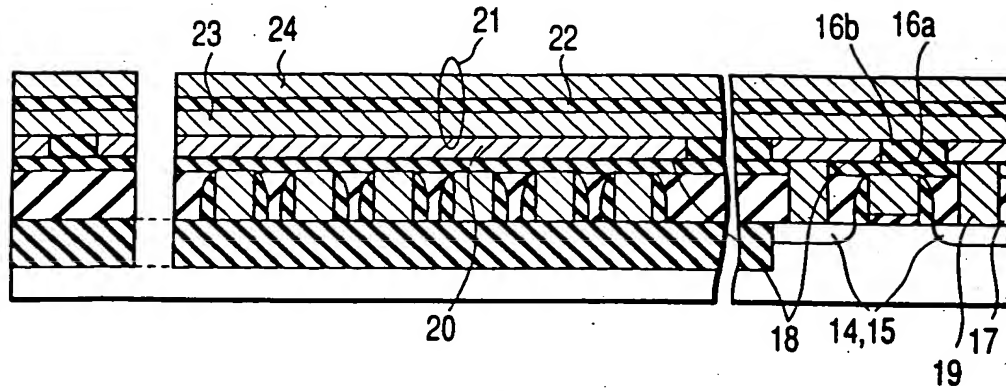


FIG. 18

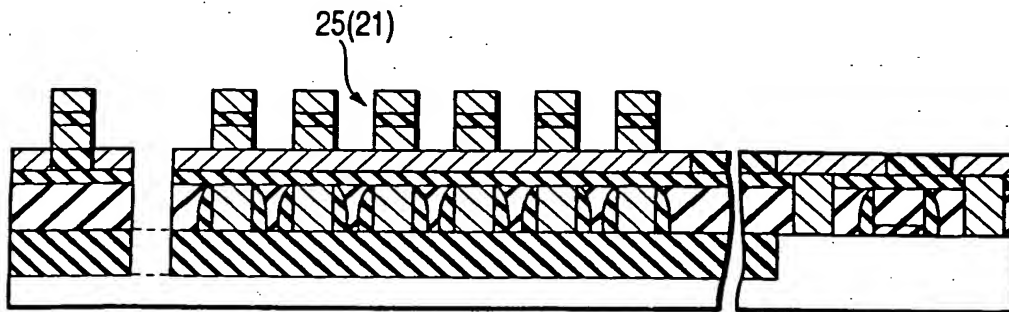


FIG. 19

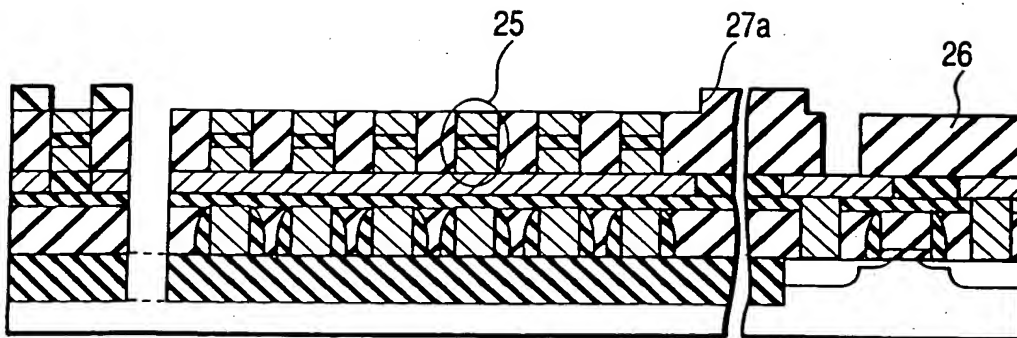


FIG. 20

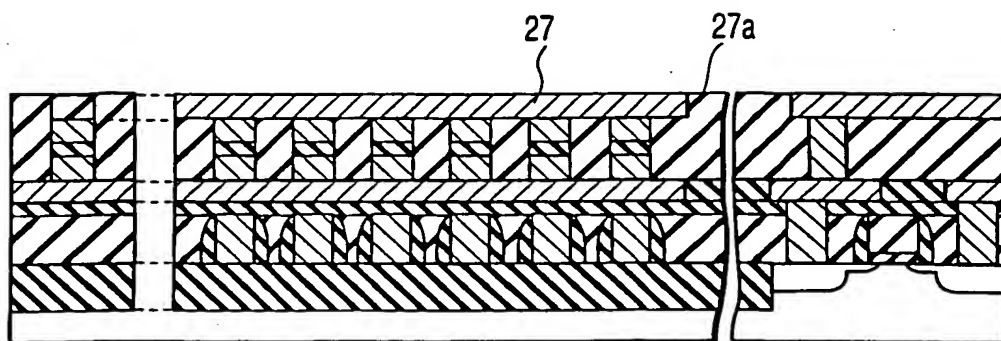


FIG. 21

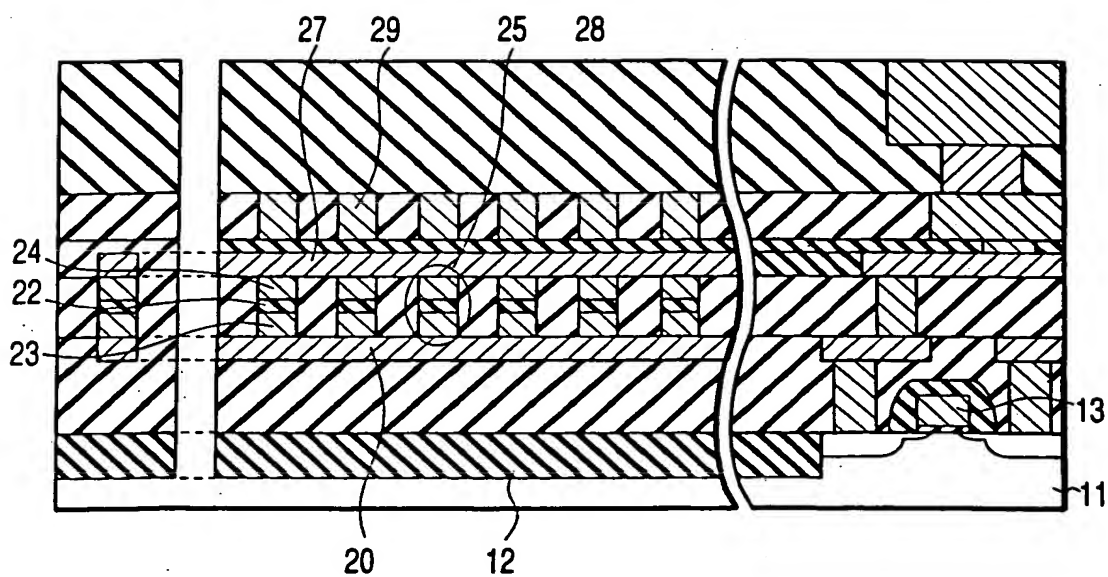


FIG. 22

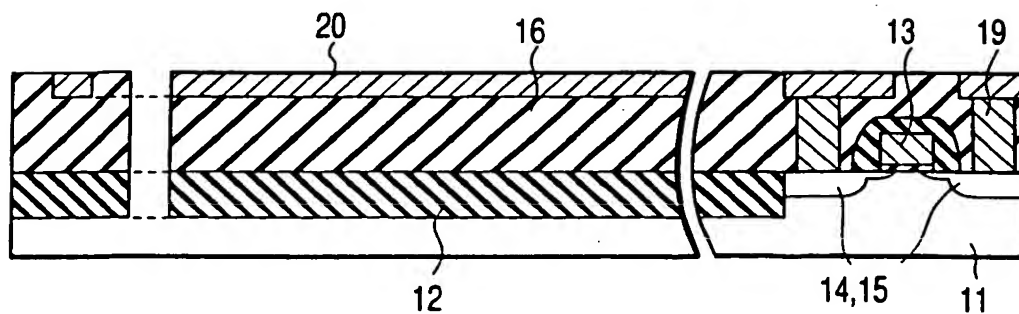


FIG. 23

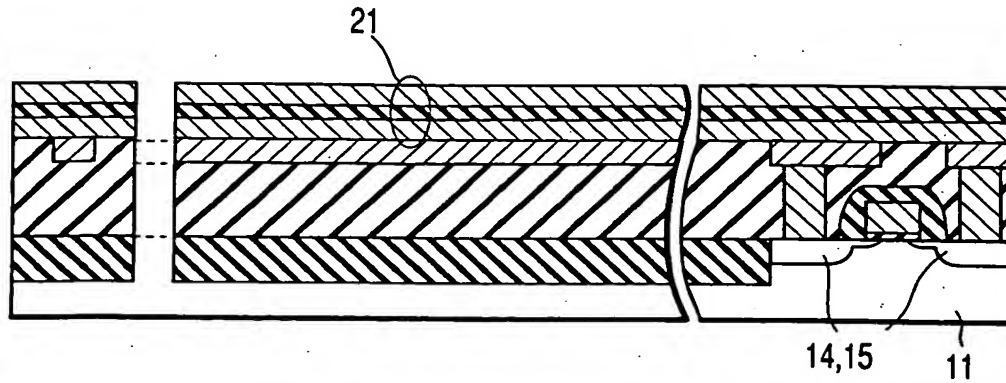


FIG. 24

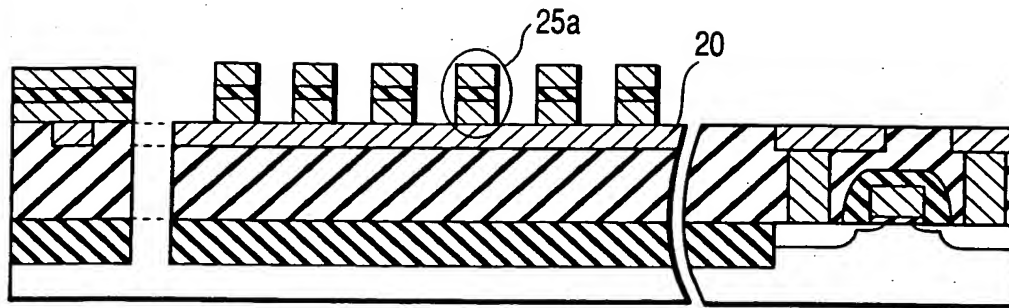


FIG. 25

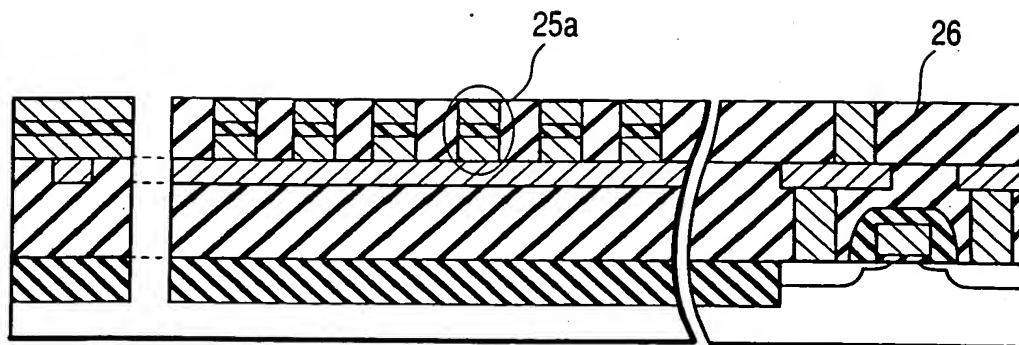


FIG. 26

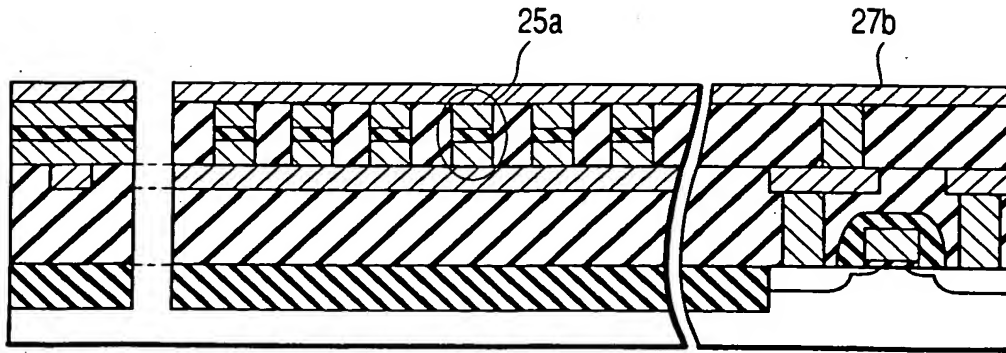


FIG. 27

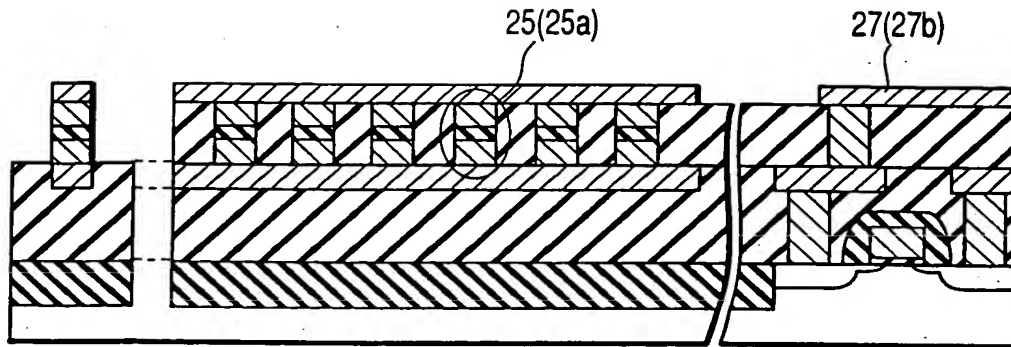


FIG. 28

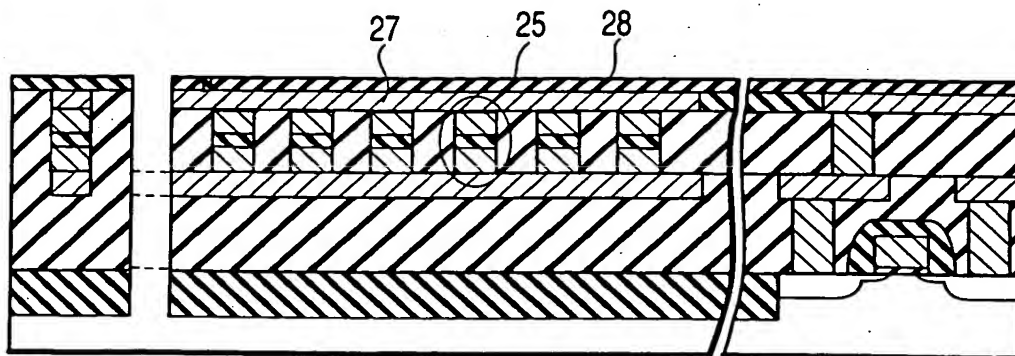


FIG. 29

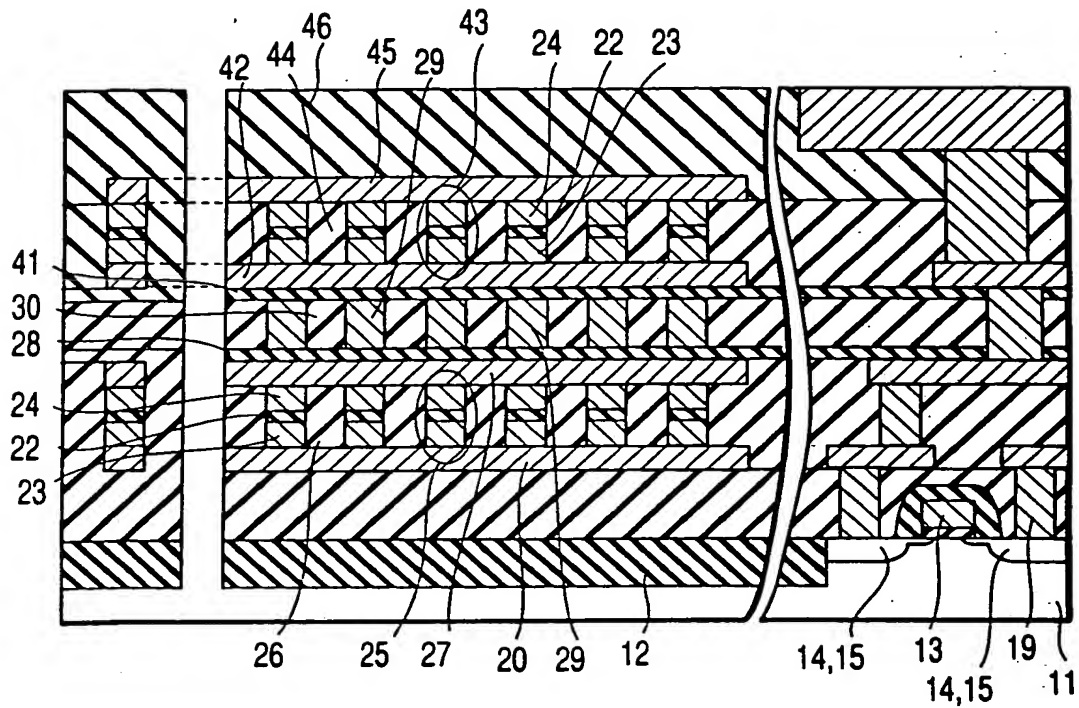


FIG. 30A

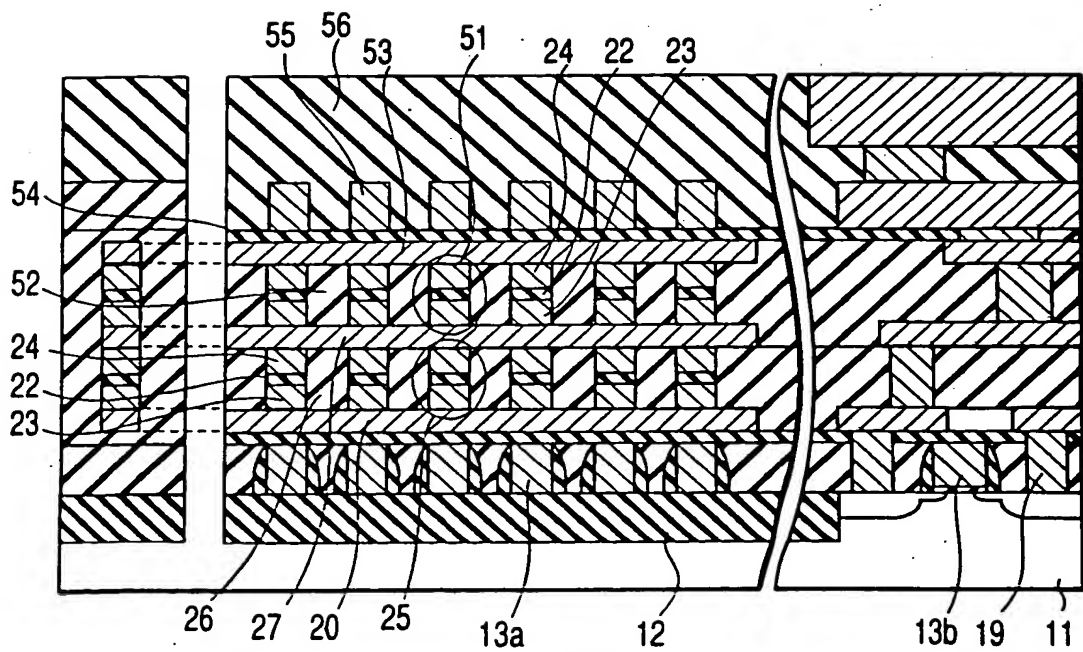


FIG. 31

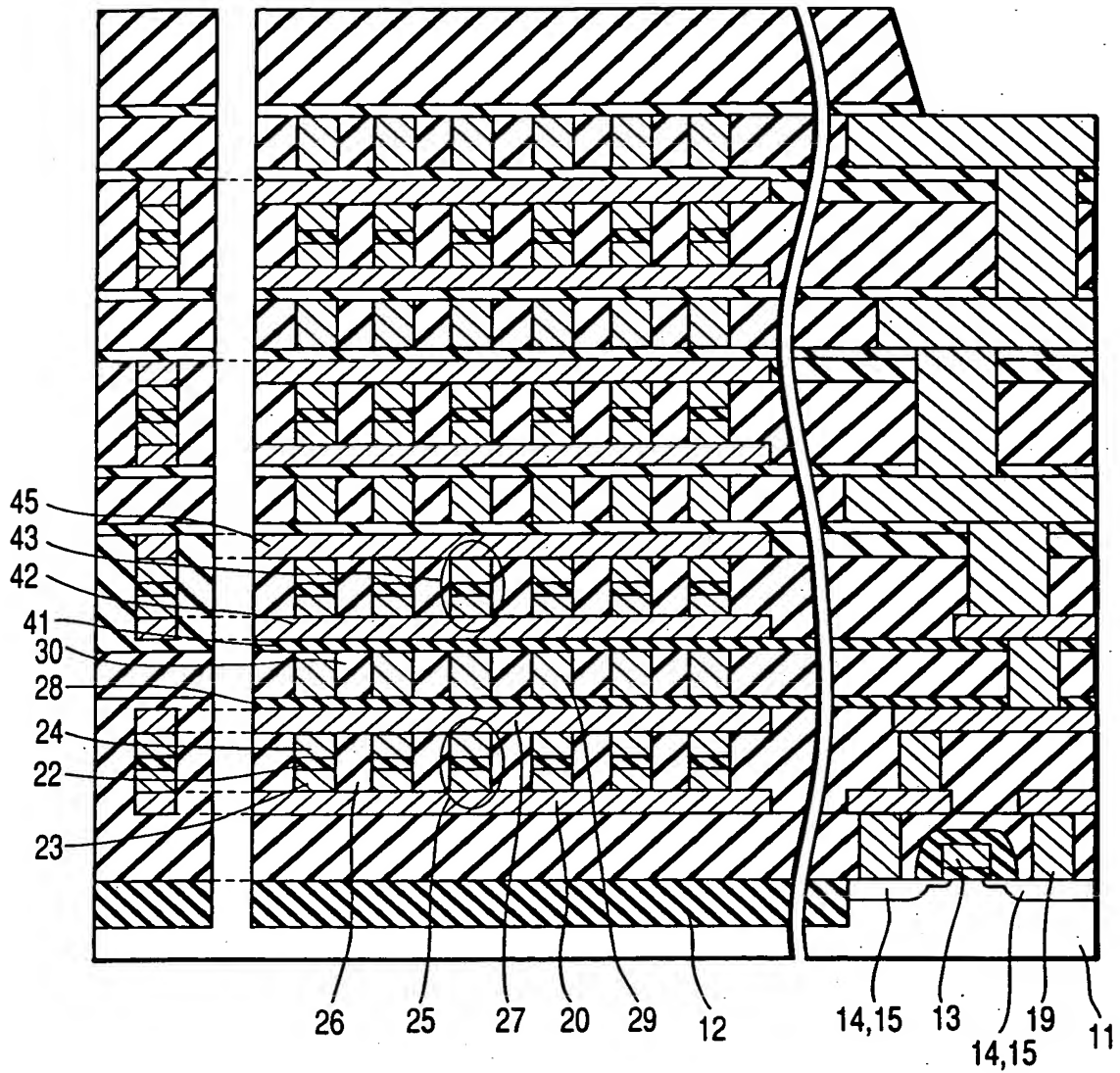


FIG. 30B

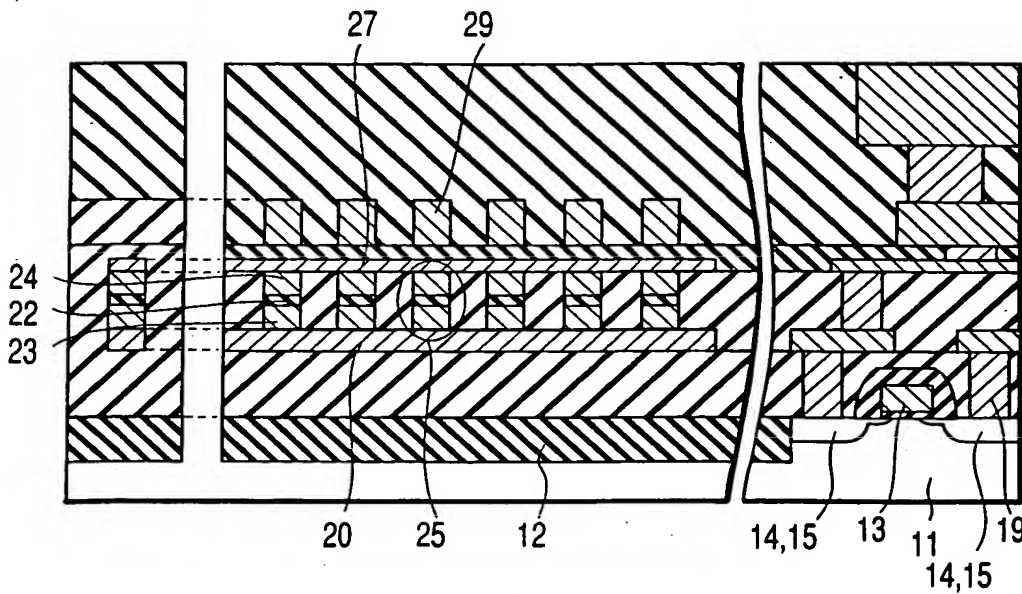


FIG. 32

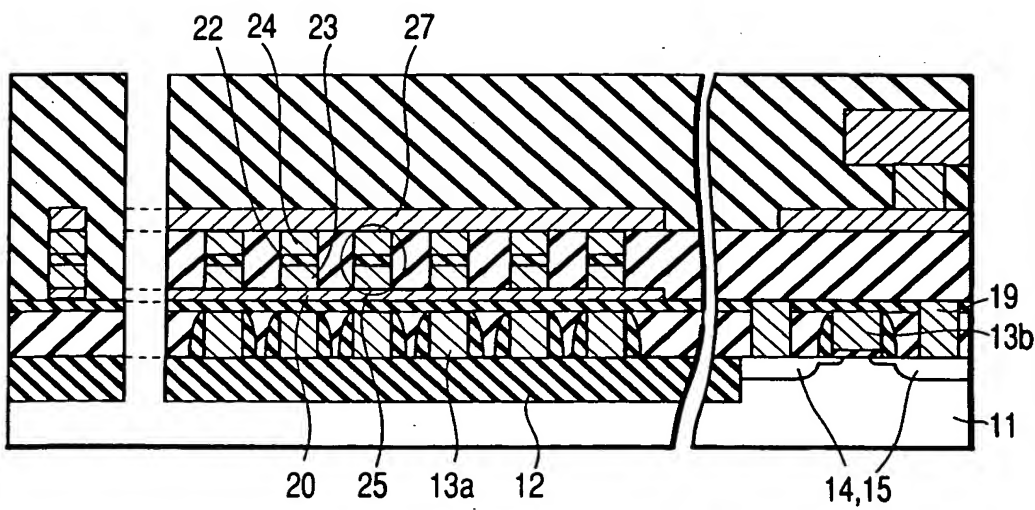


FIG. 33



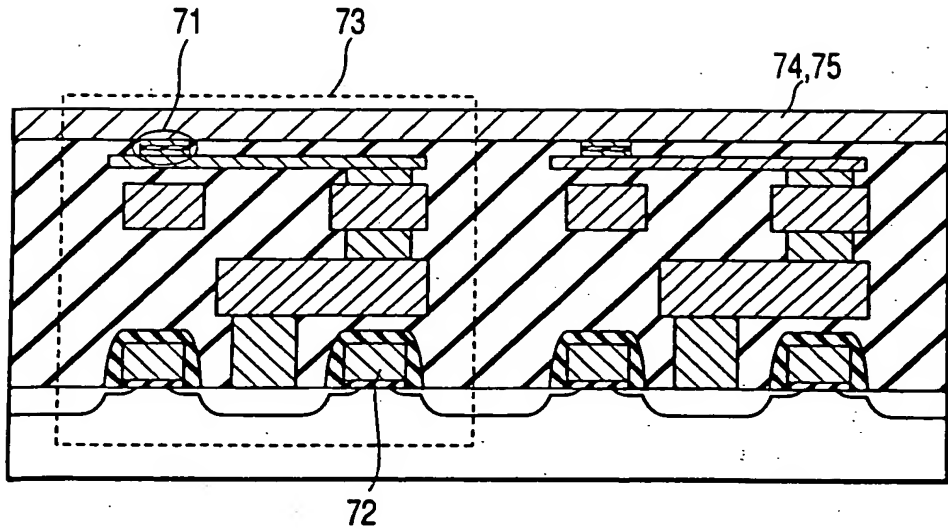


FIG. 34

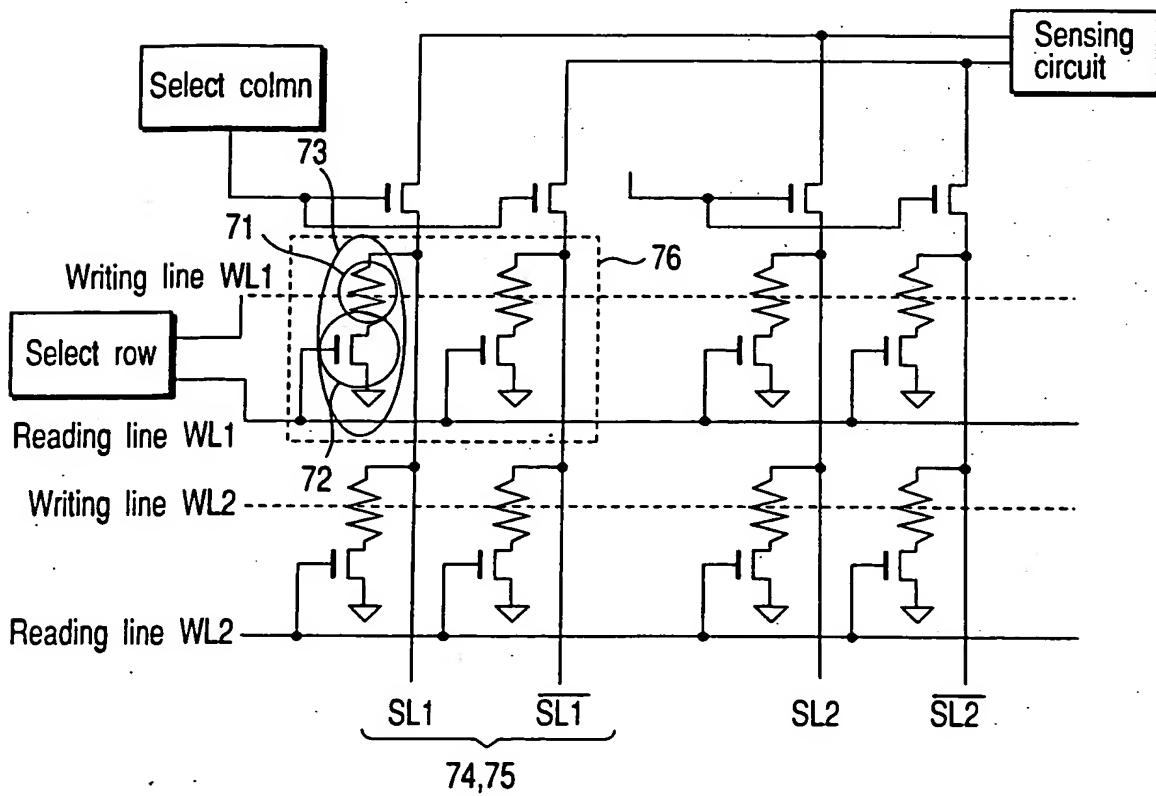


FIG. 35